Chettinad
College of Engineering & Technology
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Department of Computer Science and Engineering

CS8493 - OPERATING SYSTEMS

Unit I - MCQ Bank

1. Brain of computer is

    a. Control unit

    b. Arithmetic and Logic unit

    c. Central Processing Unit

    d. Memory

  Answer: c

2. Control Unit acts as the central nervous system of the computer.

    a. True

    b. False

  Answer: a

3. What does MBR stand for?

    a. Main Buffer Register

    b. Memory Buffer Routine

    c. Main Buffer Routine

    d. Memory Buffer Register

  Answer: d

4. In the instruction ADD A, B, the answer gets stored in

    a. B

    b. A

    c. Buffer

      d. C

Answer: b

5. What does PC stand for?

      a. Program Changer

      b. Program Counter

      c. Performance Counter

      d. Performance Changer

Answer: b

6. Which of the following holds the last instruction fetched?

      a. PC

      b. MAR

      c. MBR

      d. IR

Answer: d

7. The portion of the processor which contains the hardware required to fetch the operations is

      a. Datapath

      b. Processor

      c. Control

      d. Output unit

Answer: a

8. Causing the CPU to step through a series of micro operations is called

      a. Execution

      b. Runtime

      c. Sequencing

      d. Pipelining

Answer: c

9. The functions of execution and sequencing are performed by using

   a. Input Signals

   b. Output Signals

   c. Control Signals

   d. CPU

   Answer: c

10. What does D in the D-flip flop stand for?

   a. Digital

   b. Direct

   c. Delay

   d. Durable

   Answer: c

11. What is the high speed memory between the main memory and the CPU called?

   a. Register Memory

   b. Cache Memory

   c. Storage Memory

   d. Virtual Memory

   Answer: b

12. Cache Memory is implemented using the DRAM chips.

   a. True

   b. False

   Answer: b

13. Whenever the data is found in the cache memory it is called as

   a. HIT

   b. MISS

   c. FOUND

     d. ERROR

Answer: a

14. LRU stands for

     a. Low Rate Usage

     b. Least Rate Usage

     c. Least Recently Used

     d. Low Required Usage

Answer: c

15. When the data at a location in cache is different from the data located in the main memory, the cache is called

     a. Unique

     b. Inconsistent

     c. Variable

     d. Fault

Answer: b

16. Which of the following is not a write policy to avoid Cache Coherence?

     a. Write through

     b. Write within

     c. Write back

     d. Buffered write

Answer: b

17. Which of the following is an efficient method of cache updating?

     a. Snoopy writes

     b. Write through

     c. Write within

     d. Buffered write

Answer: a

18. In_____mapping, the data can be mapped anywhere in the Cache Memory.

    a. Associative

    b. Direct

    c. Set Associative

    d. Indirect

Answer: a

19. The number of sign bits in a 32-bit IEEE format is

    a. 1

    b. 11

    c. 9

    d. 23

Answer: a

20. The transfer between CPU and Cache is

    a. Block transfer

    b. Word transfer

    c. Set transfer

    d. Associative transfer

Answer : a

21. Computer has a built-in system clock that emits millions of regularly spaced electric pulses per called clock cycles.

    a. second

    b. millisecond

    c. microsecond

    d. minute

Answer: a

22. It takes one clock cycle to perform a basic operation.

    a. True

    b. False

Answer: a

23. The operation that does not involves clock cycles is

    a. Installation of a device

    b. Execute

    c. Fetch

    d. Decode

Answer: a

24. The number of clock cycles per second is referred as

    a. Clock speed

    b. Clock frequency

    c. Clock rate

    d. Clock timing

Answer: a

25. CISC stands for

    a. Complex Information Sensed CPU

    b. Complex Instruction Set Computer

    c. Complex Intelligence Sensed CPU

    d. Complex Instruction Set CPU

Answer: b

26. Which of the following processor has a fixed length of instructions?

    a. CISC

    b. RISC

    c. EPIC

    d. Multi-core

Answer: b

27. Processor which is complex and expensive to produce is

    a. RISC

    b. EPIC

    c. CISC

    d. Multi-core

Answer: c

28. The architecture that uses a tighter coupling between the compiler and the processor is

    a. EPIC

    b. Multi-core

    c. RISC

    d. CISC

Answer: a

29. MAR stands for

    a. Memory address register

    b. Main address register

    c. Main accessible register

    d. Memory accessible register

Answer: a

30. A circuitry that processes that responds to and processes the basic instructions that are required

to drive a computer system is

    a. Memory

    b. ALU

    c. CU

    d. Processor

Answer : b